Lab 4: MIPS Datapath for R and I-type Instructions

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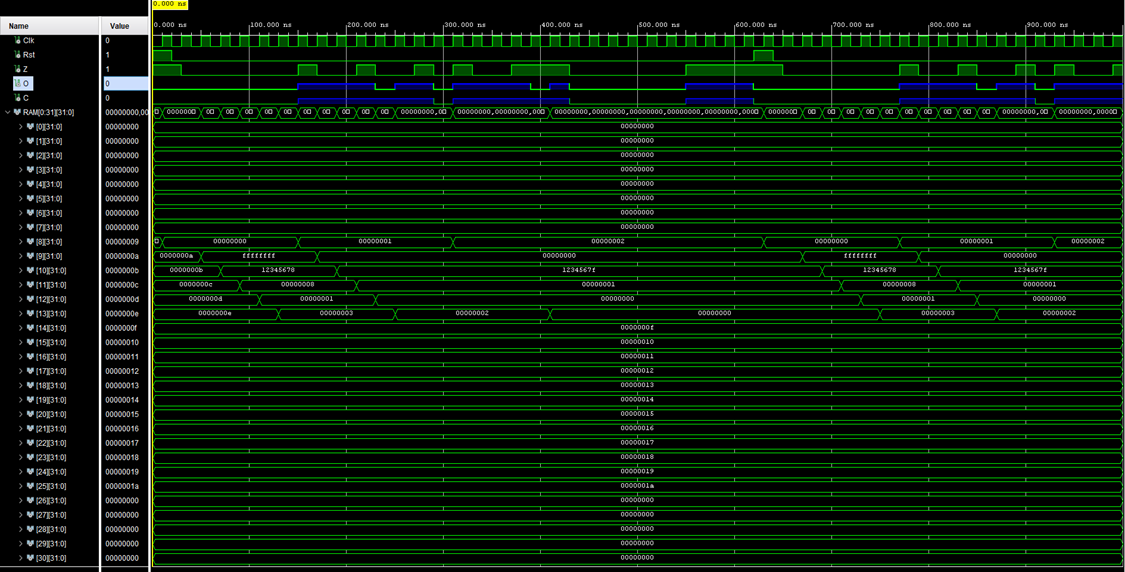
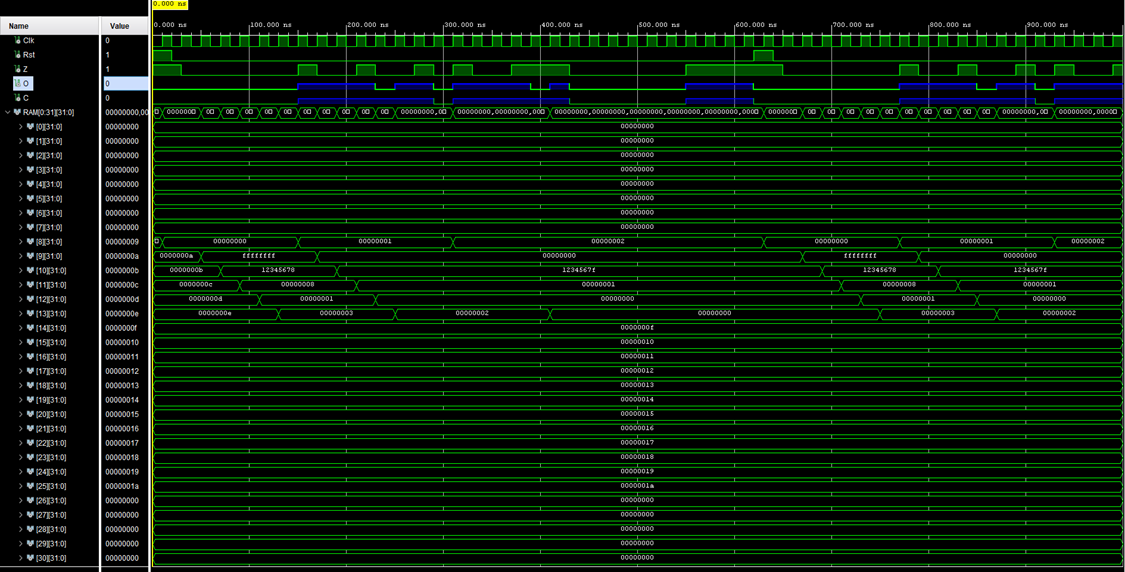
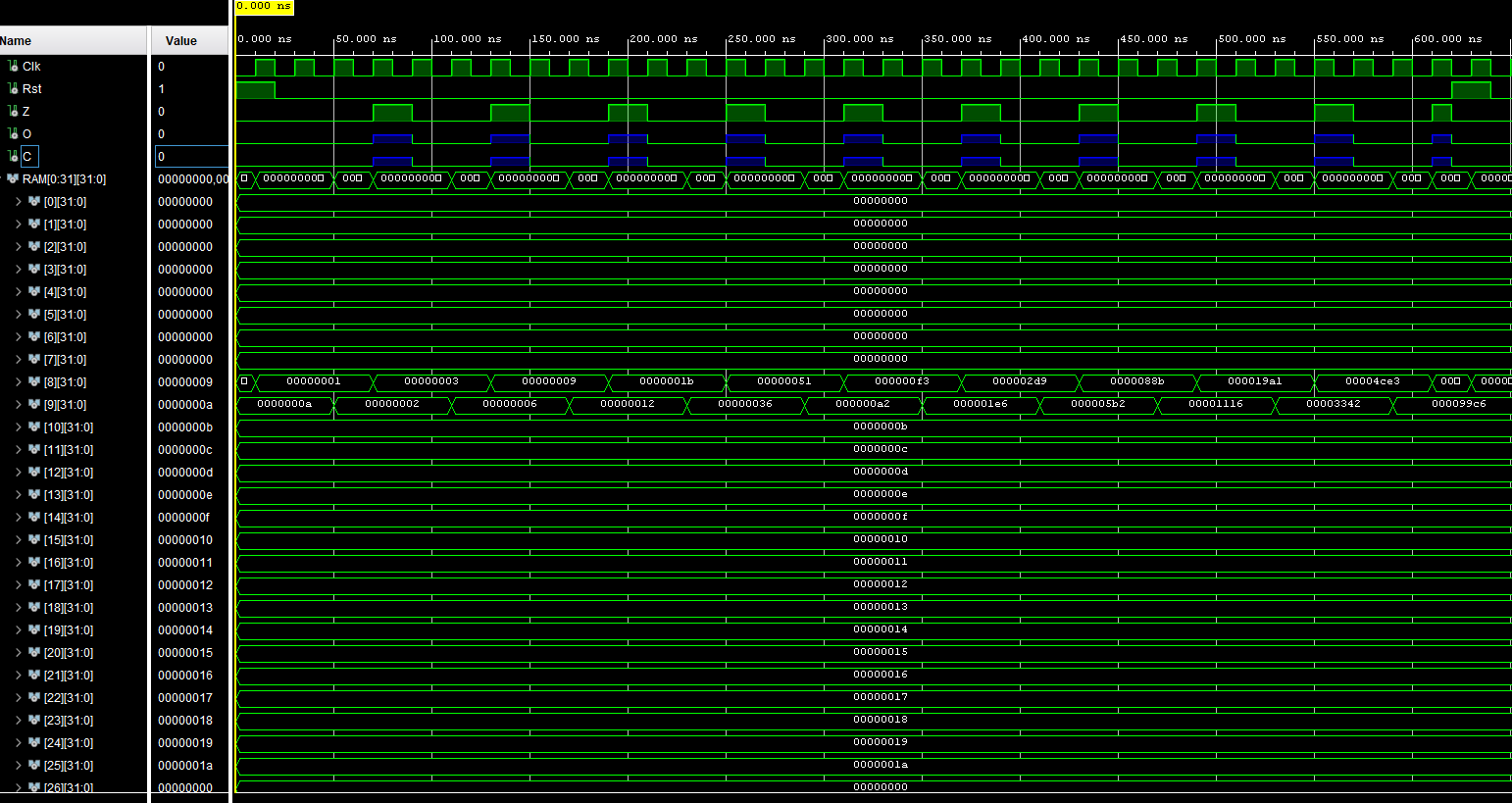
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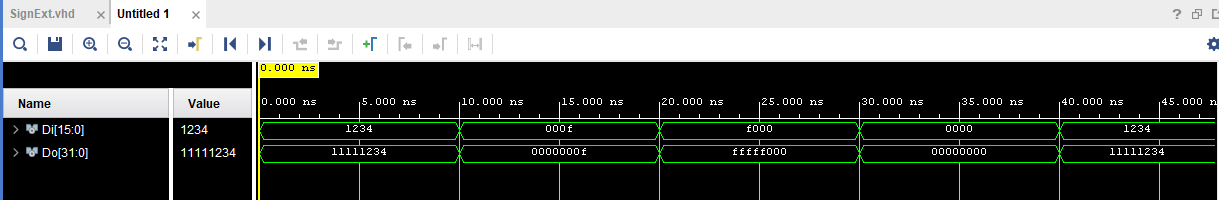
**Introduction:** The purpose of this lab is to construct a MIPS Datapath for R and I-type instructions using VHDL. The idea is to build onto the Datapath that was built during lab 3.

**Problem Logic & Solution:** Vivado’s block design tool was used to construct a block design that could process R and I-type instructions by adding a few components to accommodate for the I-type instructions.

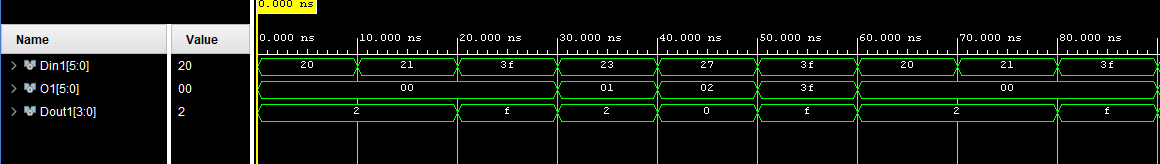
|  |  |  |
| --- | --- | --- |
| Logic Utilization | Used | |
| R-type | R and I-type |
| # of LUTs  # of Flip-Flops  # of Slices | 418  32  677 | 498  32  677 |
| Max Frequency (MHz) | 100 | 100 |

Simulation Results

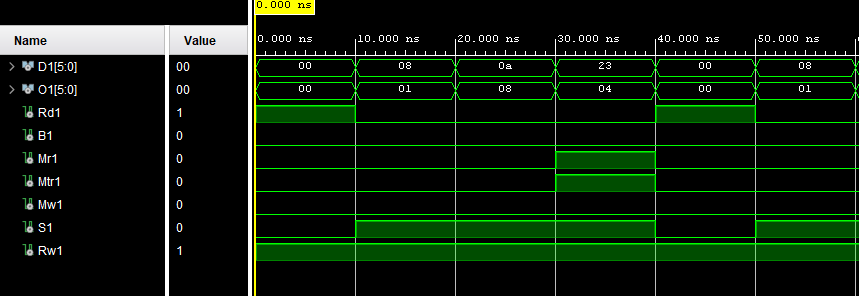
* Datapath
* MIPs Program
* SignExt



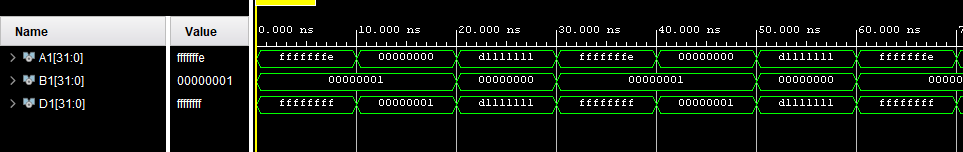
* ALUCNTL



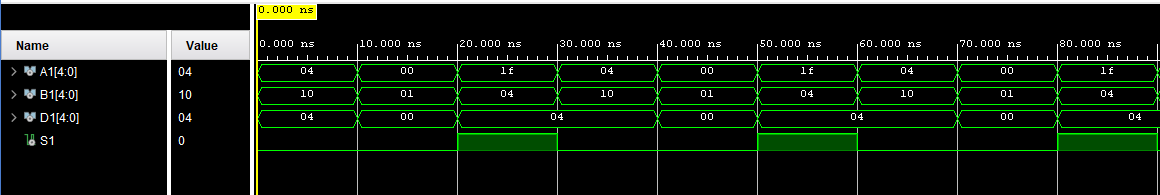
* Control



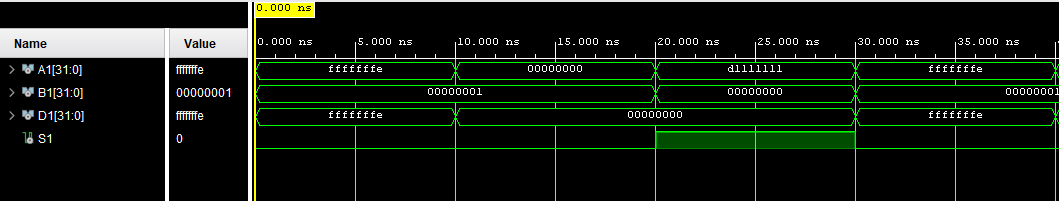
* ADD



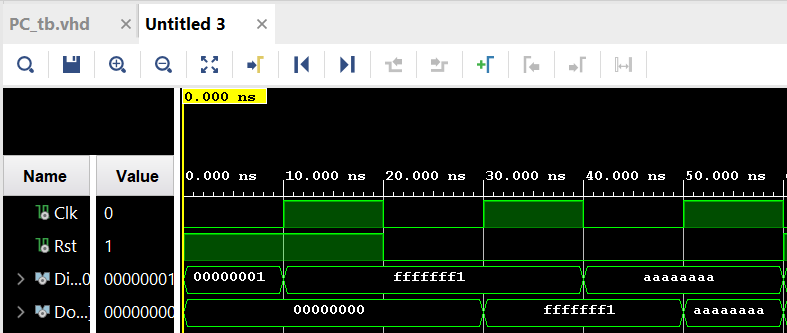
* Mux5b



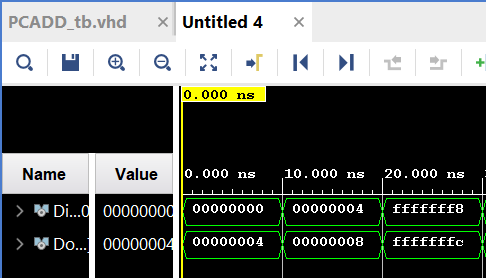
* Mux32b



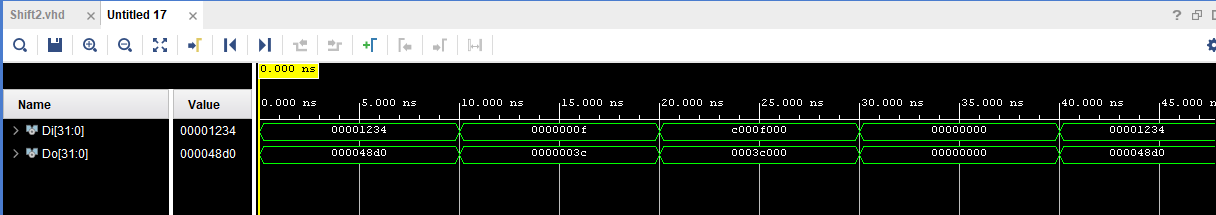
* PC



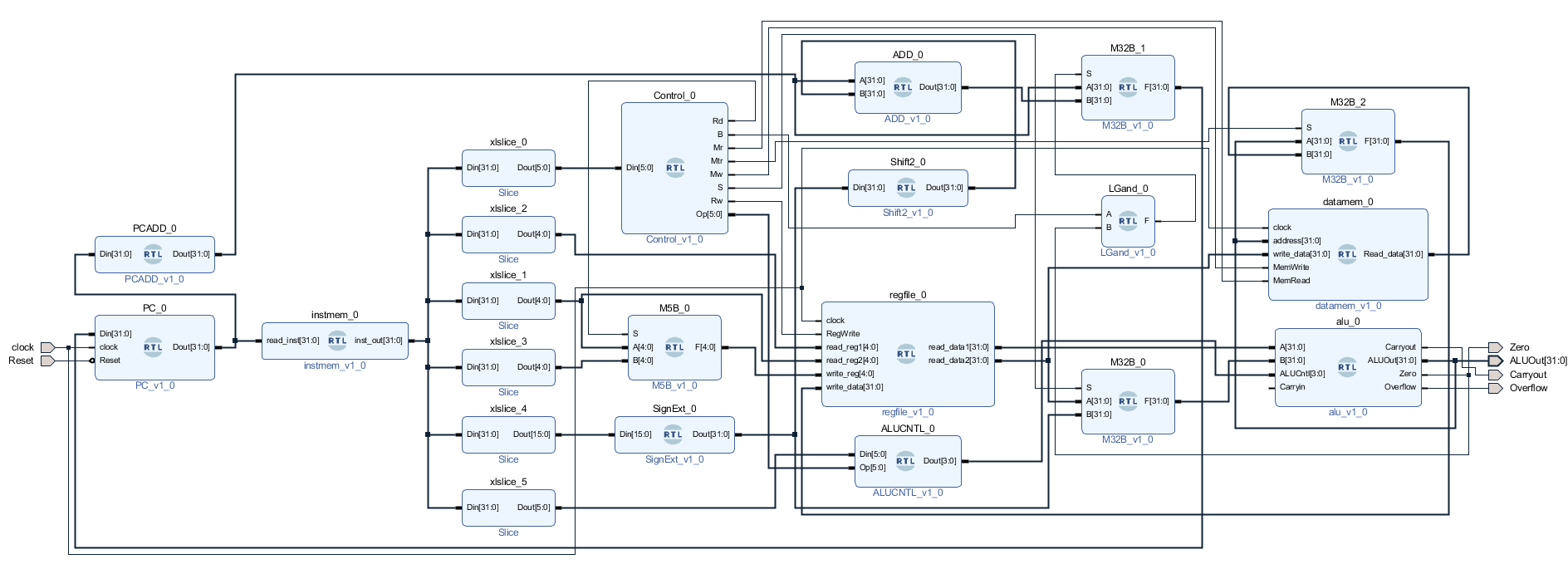
* PCADD



* Shift2



Block Design Diagram



**Conclusion:** I believe I got the correct results by looking at the simulations, this lab was not difficult the previous lab made this lab easy to understand.